

Dual Programmable Thyristor Transient Voltage Suppressor

P61089B

General Description

This device has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages.

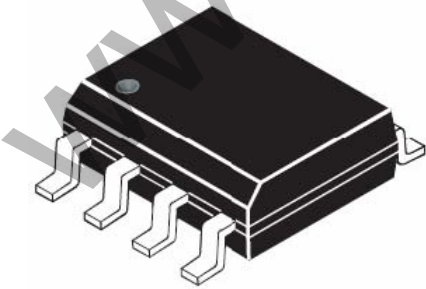
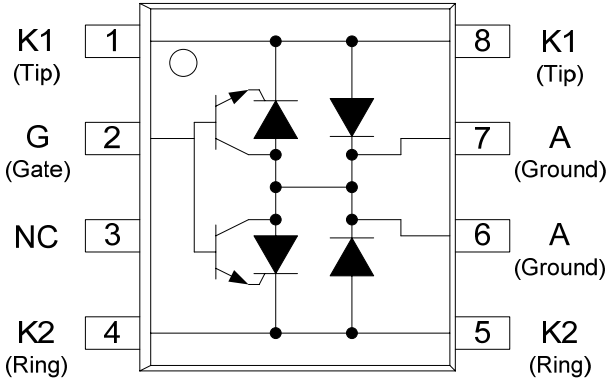
Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

This component presents a very low gate triggering current (I_{GT}) in order to reduce the current consumption on printed circuit board during the firing phase.

This devices are not subject to ageing and provide a fail safe mode in short circuit for a better protection. They are used to help equipment to meet various standards such as UL1950, IEC950/CSA C22.2, UL1459 and FCC part68.

Features

- Dual line programmable transient voltage suppressor
- Wide negative firing voltage range: $V_{MGL} = -155V$
- Holding current: $I_H > 150mA$
- Marking: H61089B
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: $I_{GT} = 5mA$ max
- Halogen Free

Package	Device Symbol
 <p>SOP-8</p>	

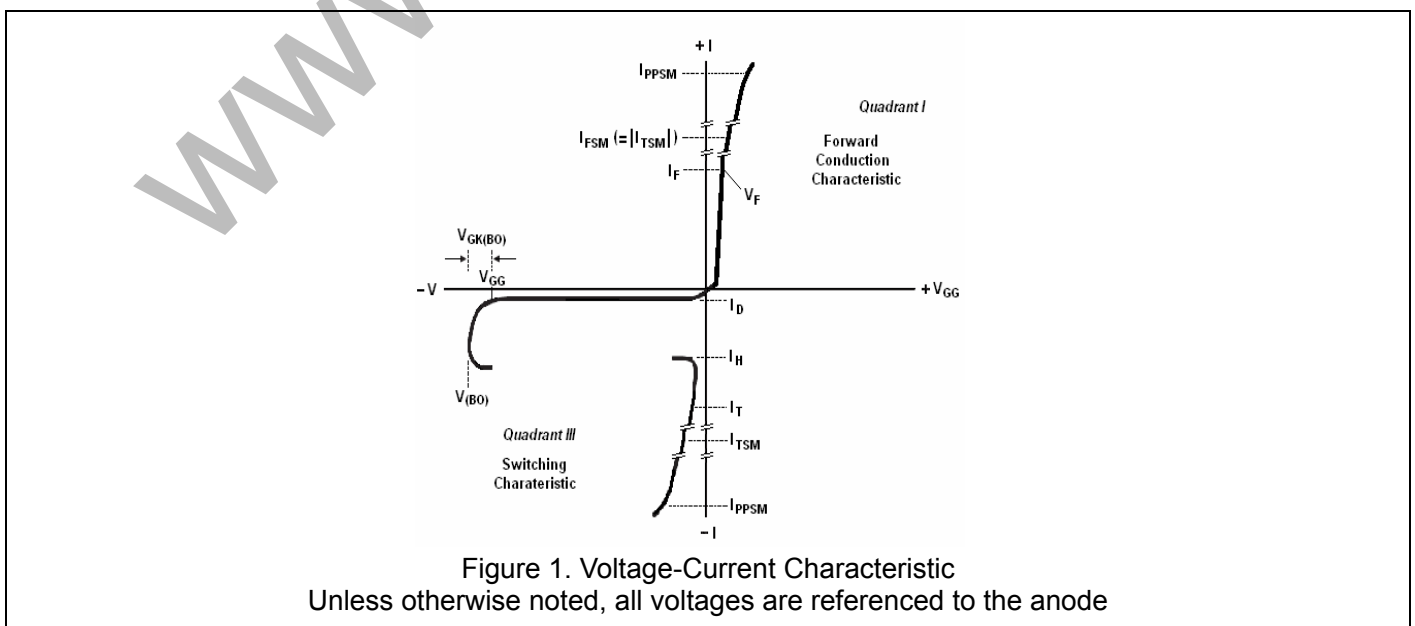
Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Repetitive peak off-state voltage, $V_{GK}=0$	V_{DRM}	-170	V
Repetitive peak gate-cathode voltage, $V_{KA}=0$	V_{GKRM}	-170	V
Non-repetitive peak on-state current 10/1000 μs (Telcordia (Bellcore) GR-1089-CORE.Issue 2.February 1999, Section4) 5/320 μs (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700 μs) 1.2/50 μs (Telcordia (Bellcore) GR-1089-CORE.Issue 2.February 1999, Section4) 2/10 μs (Telcordia (Bellcore) GR-1089-CORE.Issue 2.February 1999, Section4)	I_{PPSM}	30 40 100 120	A
Non-repetitive peak on-state current. $V_{GG}=-75\text{V}$ 50Hz to 60Hz 0.1s 1s 5s 300s 900s	I_{TSM}	11 4.8 2.7 0.95 0.93	A
Operating free-air temperature range	T_A	-40 to +85	$^\circ\text{C}$
Operating junction temperature range	T_J	-40 to +150	$^\circ\text{C}$
Storage temperature range	T_{STG}	-40 to +150	$^\circ\text{C}$
Lead soldering temperature, 10 seconds	T_{LS}	300(Mix.)	$^\circ\text{C}$

Thermal Characteristics

Parameter	Test Conditions	Max	Unit
$R_{\theta JA}$ Junction to free air thermal temperature	$T_A = 25^\circ\text{C}$, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, $P_{TOT} = 1.7\text{W}$	120	$^\circ\text{C/W}$

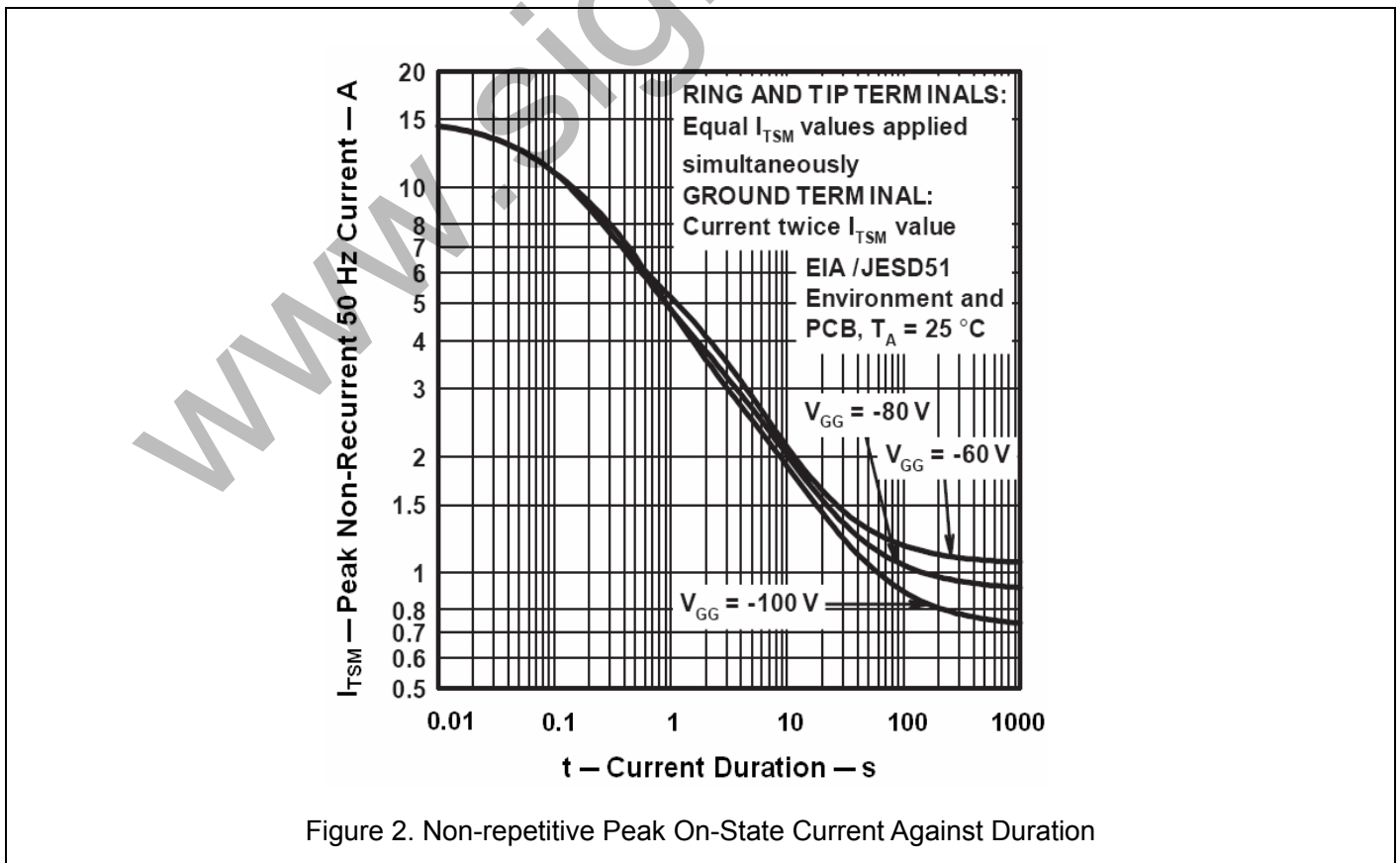
Parameter Measurement Information



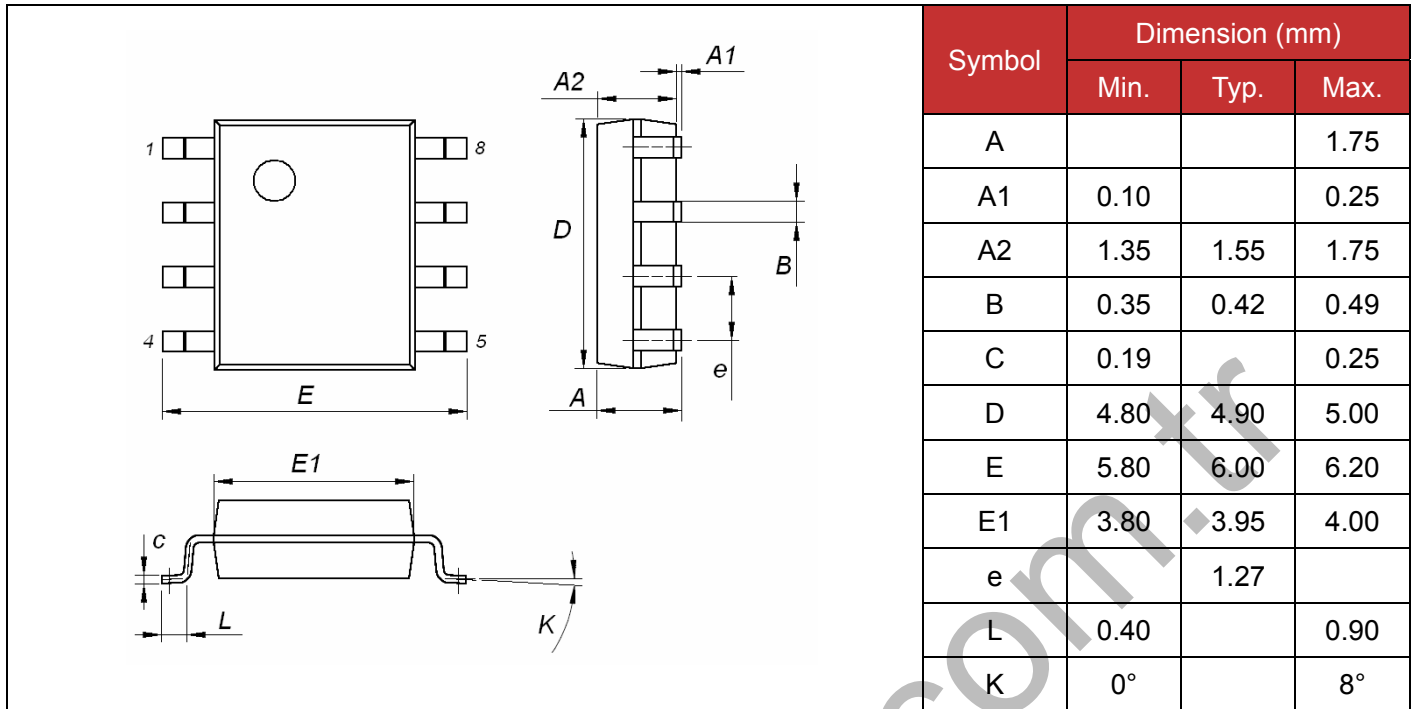
Electrical Characteristics, Rating at 25°C unless otherwise specified

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_D	Off-state current	$V_D=V_{DRM}, V_{GK}=0, V_{G2} \geq +5V$ $T_J = 25^\circ C$ $T_J = 85^\circ C$			-5 -50	μA
$V_{(BO)}$	Breakover voltage	2/10 $\mu s, I_{PP}=-56A, R_S=45\Omega, V_{GG}=-48V, C_G=220nF$ 1.2/50 $\mu s, I_{PP}=-53A, R_S=47\Omega, V_{GG}=-48V, C_G=220nF$		-57 -60		V
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 $\mu s, I_{PP}=-56A, R_S=45\Omega, V_{GG}=-48V, C_G=220nF$ 1.2/50 $\mu s, I_{PP}=-53A, R_S=47\Omega, V_{GG}=-48V, C_G=220nF$		9 12	20	V
V_F	Forward voltage	$I_F=5A, T_W=200\mu s$			3	V
V_{FRM}	Peak forward recovery voltage	2/10 $\mu s, I_{PP}=-56A, R_S=45\Omega, V_{GG}=-48V, C_G=220nF$ 1.2/50 $\mu s, I_{PP}=-53A, R_S=47\Omega, V_{GG}=-48V, C_G=220nF$		6 8		V
I_H	Holding current	$I_T=-1A, di/dt=1A/ms, V_{GG}=-48V$	-150			mA
I_{GKS}	Gate reverse current	$V_{GG}=V_{GK}=V_{GKRM}, V_{KA}=0$ $T_J = 25^\circ C$ $T_J = 85^\circ C$			-5 -50	μA
I_{GT}	Gate trigger current	$I_T=-3A, t_{p(g)} \geq 20\mu s, V_{GG}=-48V$			5	mA
V_{GT}	Gate-cathode trigger voltage	$I_T=-3A, t_{p(g)} \geq 20\mu s, V_{GG}=-48V$		2.5	4	V
Q_{GS}	Gate switching charge	1.2/50 $\mu s, I_{PP}=-53A, R_S=47\Omega, V_{GG}=-48V, C_G=220nF$		0.1		μC
C_{KA}	Cathode-anode off- state capacitance	$F=1MHz, V_D=1V, I_G=0$ $V_D=-3V$ $V_D=-48V$			100 50	pF

Typical Characteristics



Dimensions (SOP-8)



Tape Package Information

