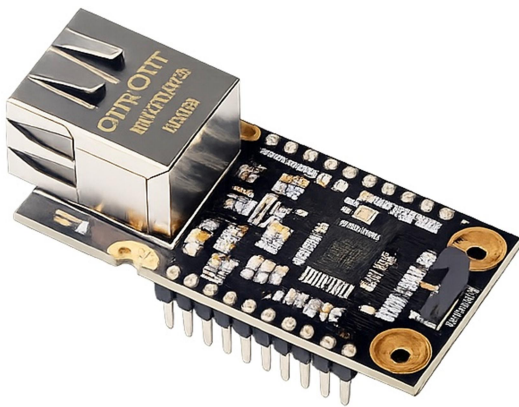
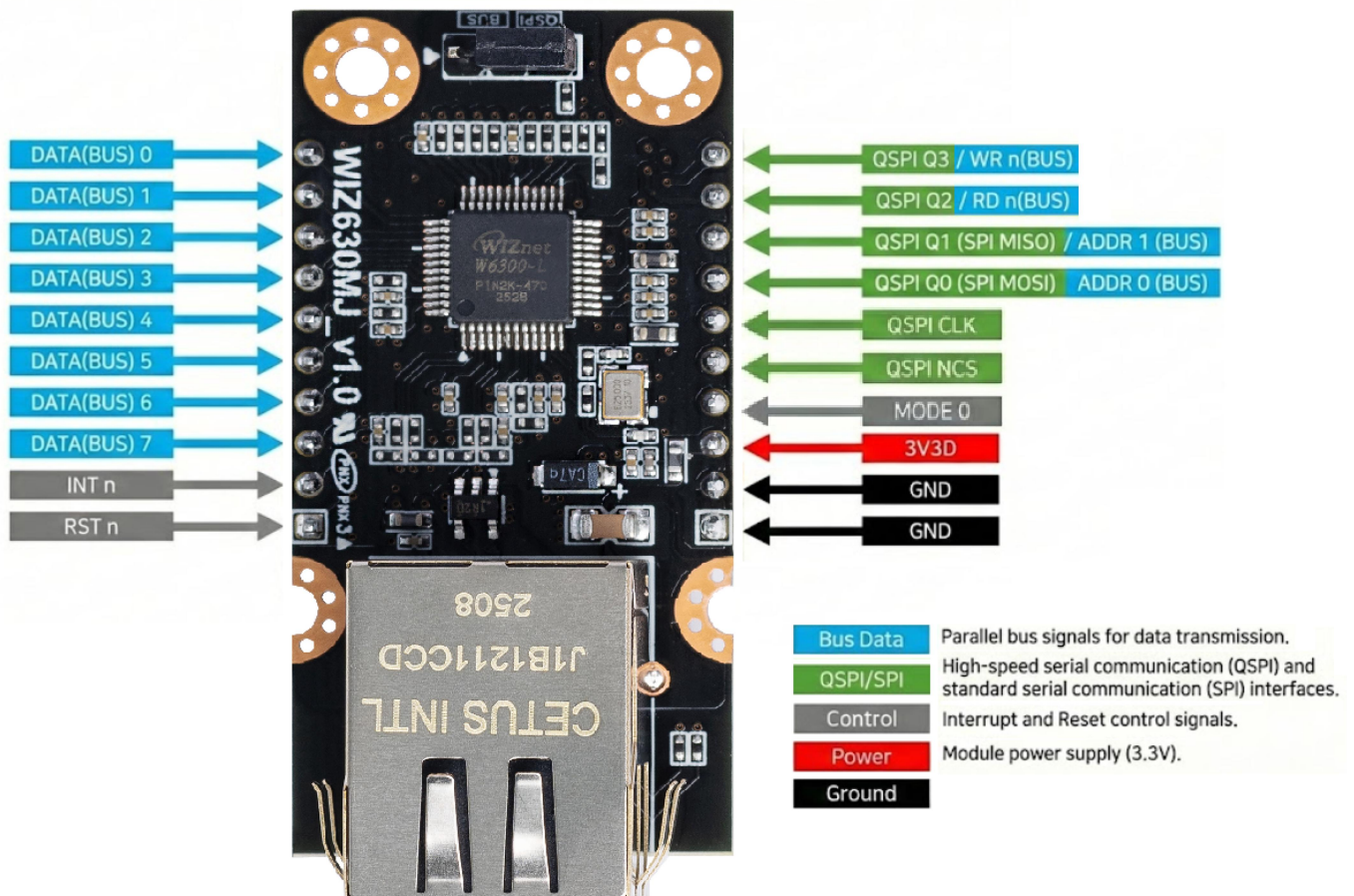


WIZ630MJ



The **WIZ630MJ** is a compact Ethernet module that integrates the **W6300** hardwired TCP/IP chip with an embedded PHY and an RJ45 MAG-JACK. It supports both **IPv4 and IPv6 Dual Stack**, enabling flexible networking for modern embedded systems. Notably, the module provides versatile host interface options by supporting both **Quad-SPI and an 8-bit bus interface**, ensuring high-speed data transmission and easy integration with various processors. By combining all essential Ethernet hardware and flexible connectivity in one module, it eliminates complex PCB design for the transformer and RJ45 interface. The WIZ630MJ is ideal for developers who want to implement network-enabled systems quickly and reliably.

WIZ630MJ Pinout



P2

Pin	Type	Name	Description
1	P	GND	Ground
2	P	GND	Ground
3	P	3V3D	3.3 V Power
4	I	MODE0	SPI/BUS Select pin SPI : Low BUS : High
5	I	SCSn	SPI Chip select (active low)
6	I	SCLK	SPI Clock input
7	I	QD0/MOSI/A0	Qual/Dual-SPI : Data 0 Single-SPI : Master-Out / Slave-In BUS : Address 0
8	O/I	QD1/MISO/A1	Qual/Dual-SPI : Data 1 Single-SPI : Master-In / Slave-Out BUS : Address 1
9	I	QD2/RDn	Qual-SPI : Data 2 BUS : indicates Read Operation
10	I	QD3/WRn	Qual-SPI : Data 3 BUS : indicates Write Operation

P3

Pin	Type	Name	Description
1	I	RSTn	Hardware reset (active low, $\geq 1 \mu s$)
2	O	INTn	Interrupt output (low-active)
3	IO	D7	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
4	IO	D6	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
5	IO	D5	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
6	IO	D4	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
7	IO	D3	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
8	IO	D2	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
9	IO	D1	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100
10	IO	D0	Data Bus pin SPI : DAT [7:0] must be floated. BUS : Data is carried over DAT [7:0] between HOST and W6100

Features

- Supports Hardwired TCP/IP protocols: TCP, UDP, IPv6, IPv4, ICMPv6, ICMPv4, IGMP, MLDv1, ARP, PPPoE
- Dual Stack IPv4/IPv6 support
- High-speed operation with 150 MHz system clock
- Up to 80 Mbps throughput via QSPI (4-bit data interface)
- 8 independent sockets with total 64 KB SRAM (4 KB TX/RX per socket)
- Supports SOCKET-less commands (ARP, ICMPv6 for DAD, NA, RS)
- Integrated transformer and RJ45 MAG-JACK
- Supports Ethernet PHY power down & clock switching for low power
- Supports Wake-on-LAN (UDP)
- High-speed Quad/Dual/Single-SPI interface (Mode 0/3)
- Parallel bus mode with 8-bit data and 2 address lines
- 10BaseT / 10Base-Te / 100BaseTX Ethernet PHY integrated
- Auto-Negotiation and Auto-MDIX supported
- 3.0 V operation (5 V I/O tolerant)
- Network LEDs for link, speed, duplex, and activity
- 2 × 10-pin headers (2.54 mm pitch)
- Selectable host interface between QSPI and 8-bit bus via on-board jumper cap
- Operating temperature: -40 °C to +85 °C

Electrical Characteristics

- DC Characteristics
- Power Dissipation

Symbol	Parameter	Pins	Min	Typ	Max	Unit
V _{DD}	Supply voltage	3.3 V	2.97	3.3	3.63	V
V _{IH}	High-level input	ALL	2.0	—	—	V
V _{IL}	Low-level input	ALL	—	—	0.8	V
V _{OH}	High-level output	ALL	2.4	3.3	—	V
V _{OL}	Low-level output	ALL	0.0	—	0.4	V
I _{DD}	Supply current (Normal)	3.3 V	—	TBD	—	mA
I _{PD}	Supply current (Power-down)	3.3 V	—	TBD	—	mA

- **Form factor:** Compact ioModule with integrated RJ45 MAG-JACK
- **Pin pitch:** 2.54 mm (2 × 10 header)
- **Dimensions:** 28.0 × 28.0 mm (typ.)